

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims of the
5 application:

Listing of claims:

1. (Currently amended) A new grid metal design for image sensors comprising:
a semiconductor image sensor chip having a pixel region covering most of the
chip and a logic circuit region on the chip periphery, the pixel region containing an
10 array of image pixels where for each image pixel the majority of its area is occupied
by a light sensing element and the other image pixel circuit elements are arranged in
the periphery of the image pixel without overlapping the image sensing element;
a number of metal levels of the first type, where at each of the levels of the first
type functional patterns exist both for the chip peripheral logic circuits and for the
15 pixel circuit elements;
a number of metal levels of the second type, where in each of said levels of the
second type functional patterns may exist only for the chip peripheral logic circuits
and dummy metal patterns cover the pixel region except for the light sensing
elements, where the total number of metal levels is at least five and there is at least
20 one level of type one and at least one level of type two;
a first dielectric layer under the first metal layer, an interlevel dielectric layer
between said metal levels of either type and a passivation layer over the last metal
level.

2. (Original) The design of Claim 1 wherein the array of image pixels is a grid matrix

array.

3. (Original) The design of Claim 1 wherein the number of metal levels of the first type is between one and four.

4. (Original) The design of Claim 1 wherein the number of metal levels of the second type is between one and four.

5. (Original) The design of Claim 1 wherein the metal levels of the first type and of the second type are composed of either copper, gold, aluminum, cobalt or tungsten or of composites of these metals or of metal silicides.

6. (Original) The design of Claim 1 wherein the dielectric and passivation levels are composed of dielectric materials such as silicon oxide, silicon nitride or silicon oxynitride.

7. (Currently amended) A method of fabricating a new grid metal design for image sensors comprising:

providing a partially processed semiconductor wafer having chips in which are partially formed image sensors, said partially formed image sensor chips having pixel regions and chip peripheral logic circuit regions, the pixel region containing an array of image pixels and where for each image pixel of a pixel region the majority of its area is occupied by a light sensing element and the other image pixel elements are arranged in the periphery of the image pixel so as not to cover the light sensing element.

forming a number of metal levels of the first type, where at each of the levels of the first type functional patterns exist both for the chip peripheral logic circuits and for the pixel circuit elements;

forming a number of metal levels of the second type, where in each of said levels of

the second type functional patterns may exist only for the chip peripheral logic

circuits and dummy metal patterns cover the pixel region except for the light sensing

elements, where the total number of metal levels is at least five and there is at least

5 one level of type one and at least one level of type two;

forming a first dielectric layer under the first metal layer, an interlevel dielectric layer between said metal levels of either type and a passivation layer over the last metal level.

8. (Original) The method of Claim 7 wherein the array of image pixels is a grid matrix
10 array.

9. (Original) The method of Claim 7 wherein the number of metal levels of the first type is between one and four.

10. (Original) The method of Claim 7 wherein the number of metal levels of the second type is between one and four.

15 11. (Original) The method of Claim 7 wherein the metal levels of the first type and of the second type are composed of either copper, gold, aluminum, cobalt or tungsten or of composites of these metals or of metal silicides.

12. (Original) The method of Claim 7 wherein the dielectric and passivation levels are composed of

20 dielectric materials such as silicon oxide, silicon nitride or silicon oxynitride.

13. (Currently amended) A new grid metal design for CMOS image sensors comprising:

a semiconductor image sensor chip having a pixel region covering most of the chip and a logic circuit region on the chip periphery, the pixel region containing an array of image pixels where for each image pixel the majority of its area is occupied by a light sensing element and the other image pixel circuit elements are arranged in the periphery of the image pixel without overlapping the image sensing element;

a number of metal levels of the first type, where at each of the levels of the first type functional patterns exist both for the chip peripheral logic circuits and for the pixel circuit elements;

a number of metal levels of the second type, where in each of said levels of the second type functional patterns may exist only for the chip peripheral logic circuits and dummy metal patterns cover the pixel region except for the light sensing elements, where the total number of metal levels is at least five and there is at least one level of type one and at least one level of type two;

a first dielectric layer under the first metal layer, an interlevel dielectric layer between said metal levels of either type and a passivation layer over the last metal level.

14. (Original) The design of Claim 13 wherein the light sensing element is a photodiode.

15. (Original) The design of Claim 13 wherein the array of image pixels is a grid matrix array.

16. (Original) The design of Claim 13 wherein the number of metal levels of the first type is between one and four.

17. (Original) The design of claim 13 wherein the number of metal levels of the second type is between one and four.

18. (Original) The design of Claim 13 wherein the metal levels of the first type and of the

second type are composed of either copper, gold, aluminum, cobalt or tungsten or of composites of these metals or of metal silicides.

5 19. (Original) The design of Claim 13 wherein the dielectric and passivation levels are composed of

dielectric materials such as silicon oxide, silicon nitride or silicon oxynitride.

20. (Currently amended) A method of fabricating a new grid metal design for CMOS image sensors comprising:

providing a partially processed semiconductor wafer having chips in which are

10 partially formed image sensors, said partially formed image sensor chips having pixel regions and chip peripheral logic circuit regions, the pixel region containing an array of image pixels and where for each image pixel of a pixel region the majority of its area is occupied by a light sensing element and the other image pixel elements are arranged in the periphery of the image pixel so as not to cover the light sensing element.

15 forming a number of metal levels of the first type, where at each of the levels of the first type functional patterns exist both for the chip peripheral logic circuits and for the pixel circuit elements;

forming a number of metal levels of the second type, where in each of said levels of the second type functional patterns may exist only for the chip peripheral logic

20 circuits and dummy metal patterns cover the pixel region except for the light sensing elements, where the total number of metal levels is at least five and there is at least one level of type one and at least one level of type two;

forming a first dielectric layer under the first metal layer, an interlevel dielectric layer between said metal levels of either type and a passivation layer over the last metal level.

21. (Original) The method of Claim 20 wherein the light sensing element is a photodiode.

22. (Original) The method of Claim 20 wherein the array of image pixels is a grid matrix array.

23. (Original) The method of Claim 20 wherein the number of metal levels of the first type is between one and four.

24. (Original) The method of Claim 20 wherein the number of metal levels of the second type is between one and four.

25. (Original) The method of Claim 20 wherein the metal levels of the first type and of the second type are composed of either copper, gold, aluminum, cobalt or tungsten or of composites of these metals or of metal silicides.

26. (Original) The method of Claim 20 wherein the dielectric and passivation levels are composed of dielectric materials such as silicon oxide, silicon nitride or silicon oxynitride.

27. (Currently amended) A new grid metal design for bipolar image sensors comprising:

a semiconductor image sensor chip having a pixel region covering most of the chip and a logic circuit region on the chip periphery, the pixel region containing an array of image pixels where for each image pixel the majority of its area is occupied

by a light sensing element and the other image pixel circuit elements are arranged in

the periphery of the image pixel without overlapping the image sensing element;

a number of metal levels of the first type, where at each of the levels of the first type functional patterns exist both for the chip peripheral logic circuits and for the pixel circuit elements;

a number of metal levels of the second type, where in each of said levels of the second type functional patterns may exist only for the chip peripheral logic circuits and dummy metal patterns cover the pixel region except for the light sensing elements, where the total number of metal levels is at least five and there is at least one level of type one and at least one level of type two;

a first dielectric layer under the first metal layer, an interlevel dielectric layer between said metal levels of either type and a passivation layer over the last metal level.

28. (Original) The design of Claim 27 wherein the light sensing element is an emitter-base junction of a bipolar transistor.

29. (Original) The design of Claim 27 wherein the array of image pixels is a grid matrix array.

30. (Original) The design of Claim 27 wherein the number of metal levels of the first type is between one and four.

31. (Original) The design of claim 27 wherein the number of metal levels of the second type is between one and four.

32. (Original) The design of Claim 27 wherein the metal levels of the first type and of the

second type are composed of either copper, gold, aluminum, cobalt or tungsten or of composites of these metals or of metal silicides.

33. (Original) The design of Claim 27 wherein the dielectric and passivation levels are

5 composed of

dielectric materials such as silicon oxide, silicon nitride or silicon oxynitride.

34. (Currently amended) A method of fabricating a new grid metal design for bipolar

image sensors comprising:

providing a partially processed semiconductor wafer having chips in which are

10 partially formed image sensors, said partially formed image sensor chips having pixel regions and chip peripheral logic circuit regions, the pixel region containing an array of image pixels and where for each image pixel of a pixel region the majority of its area is occupied by a light sensing element and the other image pixel elements are arranged in the periphery of the image pixel so as not to cover the light sensing element.

15 forming a number of metal levels of the first type, where at each of the levels of the first type functional patterns exist both for the chip peripheral logic circuits and for the pixel circuit elements;

forming a number of metal levels of the second type, where in each of said levels of the second type functional patterns may exist only for the chip peripheral logic

20 circuits and dummy metal patterns cover the pixel region except for the light sensing elements, where the total number of metal levels is at least five and there is at least

one level of type one and at least one level of type two;

forming a first dielectric layer under the first metal layer, an interlevel dielectric layer between said metal levels of either type and a passivation layer over the last metal level.

35. (Original) The method of Claim 34 wherein the light sensing element is an emitter-
5 base junction of a bipolar transistor.

36. (Original) The method of Claim 34 wherein the array of image pixels is a grid matrix array.

37. (Original) The method of Claim 34 wherein the number of metal levels of the first type is between one and four.

10 38. (Original) The method of Claim 34 wherein the number of metal levels of the second type is between one and four.

39. (Original) The method of Claim 34 wherein the metal levels of the first type and of the second type are composed of either copper, gold, aluminum, cobalt or tungsten or of composites of these metals or of metal silicides.

15 40. (Original) The method of Claim 34 wherein the dielectric and passivation levels are composed of dielectric materials such as silicon oxide, silicon nitride or silicon oxynitride.

Amendments to the drawings

The following amendments are made to correct the drawings:

5 In Figs. 4 and 6 the reference sign “28” had been inappropriately used, since it is already used otherwise, to designate a photodiode. In the amended Figs. 4 and 6 the photodiode is designated by the reference sign “70”.

Fig. 6 has been amended to show a logic circuit region on the chip periphery and a number of metal levels of the first type.